



MADANAPALLE INSTITUTE OF TECHNOLOGY & SCIENCE
(UGC-AUTONOMOUS INSTITUTION)

Affiliated to JNTUA, Ananthapuramu & Approved by AICTE, New Delhi
NAAC Accredited with A+ Grade, NIRF India Rankings 2025 - Band: 201-300 (Engg.)
NBA Accredited - B.Tech. (CIVIL, CSE, CST, ECE, EEE, MECH), MBA & MCA
www.mits.ac.in



Examination Branch

M. Tech (VLSI Design & Embedded Systems) – I Year II Semester (R24) Supplementary End Semester Examinations January-2026

(For 2024 Admitted batch)

TIME TABLE

Academic Year: 2025– 26

Time: 02:00 PM to 05:00 PM

Duration: 3 hours

DATE / DAY	Course Name & Code
19.01.2026 (Monday)	CMOS Analog IC Design-24VES103
20.01.2026 (Tuesday)	Embedded System Design-24VES104
21.01.2026 (Wednesday)	Pattern Recognition and Machine Learning-24VES107
22.01.2026 (Thursday)	Physical Design Automation-24VES112

Note: (i) Any clashes or omissions in the time table may please be informed to the Controller of Examinations Immediately.
(ii) Even if Government declares holiday on any of the above dates, the examination shall be conducted as usual.

Ge Natesh - L. mudi
CONTROLLER OF EXAMINATIONS
MADANAPALLE INSTITUTE OF TECHNOLOGY & SCIENCE

Date: 05.01.2026

Copy to: Madanapalle Institute of

1. ECE HOD
2. Transport Incharge
3. Notice Board (AS & Dept)
4. File (AS)

P. Ranjith
PRINCIPAL

Principal
Madanapalle Institute of
Technology & Science
MITS